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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/694,913	10/29/2003	Gen Sasaki	244176US2 DIV	4521

22850 7590 11/19/2007

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EXAMINER	
TRAN, NHAN T	

ART UNIT	PAPER NUMBER
2622	

NOTIFICATION DATE	DELIVERY MODE
11/19/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/694,913	SASAKI, GEN	
	Examiner	Art Unit	
	Nhan T. Tran	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 September 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15,16 and 28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15,16 and 28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 15, 16 & 28 have been considered but are moot in view of the new ground of rejection.

Claim Objections

2. Claims 15 & 28 are objected to because of the following informalities:

Regarding claim 15, in line 10 of this claim, the words "and stores the defective addresses" shoud be corrected to read as -- and to store defective pixel addresses --. Furthermore, the word "separate" in lines 12 of this claim should be corrected to read as -- separately --.

Regarding claim 28, in line 7 of this claim, the word "separate" should be corrected to read as -- separately --. Furthermore, the words "said real processing" in line 19 of this claim (on page 4) should be corrected to read as -- said real time processing --.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 15, 16 & 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kosugi (US 6,426,771) in view of Fukushima et al. (US 4,893,185).

Regarding claim 15, Kosugi discloses an image processing circuit of an image input device (Figs. 1 & 2) which performs a predetermined image processing of an image photographed by an image pickup device (CCD 3) having a pixel array in said image input device (see col. 1, lines 6-12 and col. 3, lines 6-32), said circuit comprising:

a real time processing unit (DSP 6 shown in Fig. 2 and details shown in Fig. 1) in which a predetermined general image processing (i.e., color processing, JPEG processing, gamma correction, etc.) of a pixel data in the image photographed by said image pickup device and inputted sequentially is performed by real time processing (Figs. 1 & 2 and col. 3, line 52 – col. 4, line 9);

a main memory (DRAM 10) disposed outside of said real time processing unit, and configured to interchange data with the real time processing unit by direct memory access (DMA by DMA controller 7) and to store a pixel data outputted from at least said real time processing unit, in image frame units (see Figs. 1 & 2; col. 3, lines 6-32; col. 4, lines 26-30 and col. 8, line 43 – col. 15 and col. 11, lines 1-19);

a central processing unit (CPU 8) disposed separately from the real time processing unit, and configured to provide exceptional image processing (processing the image to form an image file that includes image parameters and attributes) not

including the general image processing (col. 15, line 1 - col. 16, line 67 and col. 3, lines 26-32 and note that the CPU 8 is the central processing unit that executes programs stored in the local RAM and ROM to form structure of image file).

Kosugi does not teach that the memory also stores defective pixel addresses in a pixel array sequence order having an order of the pixel array in said image input device, and said real time processing unit further comprises a defective pixel compensation block that reads the defective pixel addresses stored in said main memory arranged in the pixel array sequence order, and performs defective pixel compensation when a pixel address of a pixel data residing in the image matches said defective pixel address, said defective pixel compensation performed in the pixel array sequence order, and said defective pixel compensation block of said real time processing unit comprises a shift register with a plurality of registers connected in series, to which the defective pixel addresses stored in said memory are inputted sequentially and outputted sequentially.

However, as taught by Fukushima, an imaging apparatus is implemented with a defective pixel compensation block as a part of real time processing unit (Fig. 2) to correct defective pixels from the image sensor, wherein defective pixel addresses are stored in a memory in a pixel array sequence order having an order of the pixel array in image input device (abstract and col. 1, lines 61-67; col. 2, lines 30-33 and col. 3, lines 47-52). Fukushima also teaches that the defective pixel compensation block (combined circuits of 14 and circuits within loop 1154 in Fig. 2) that reads the defective pixel addresses stored in the memory arranged in the pixel array sequence order, and performs defective pixel compensation when a pixel address of a pixel data residing in

the image matches said defective pixel address, the defective pixel compensation performed in the pixel array sequence order (see col. 3, line 13 - col. 4, line 40), and the defective pixel compensation block of said real time processing unit comprises a shift register with a plurality of registers (101-106) connected in series, to which the defective pixel addresses stored in said memory are inputted sequentially and outputted sequentially (see Fig. 2 and col. 3, line 28 - col. 4, line 40).

Therefore, it would have been obvious to one of ordinary skill in the art to combine teachings of Kosugi and Fukushima to arrive at the Applicant's claimed invention so that any defective pixels output from the image sensor would be smoothly corrected, thereby enhancing image quality as suggested by Fukushima in col. 1, lines 9-15 and col. 2, lines 6-10.

Regarding claim 16, in the combination of Kosugi and Fukushima, Fukushima further discloses that the defective pixel compensation block comprises: a comparator (108-110 shown in Fig. 2) connected to a rearmost stage of said shift register (101-106) in which an address count value of a pixel data inputted sequentially is compared with a defective pixel address provided from said rearmost stage and, when a match is found, a defective pixel timing signal is outputted, said shift register holds a defective pixel address, and output of said rearmost stage is looped (loop back at 106) to an input terminal of a foremost stage, said comparator is a comparator in which an address count value of a pixel data inputted sequentially is compared with a defective pixel address provided from said rearmost stage and, when a match is found, a shift timing

signal and a defective pixel timing signal are outputted, and shift of said shift register is executed by said shift timing signal (shift enable signal 1154) provided from said comparator (by virtue of the flip-flop 142; see Fukushima, Fig. 2 and col. 3, line 28 - col. 5, line 14).

Regarding claim 28, all limitations of claim 28 are also met by the analyses of claims 15 & 16.

Conclusion

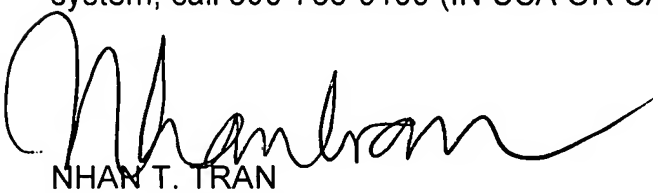
4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nhan T. Tran whose telephone number is (571) 272-7371. The examiner can normally be reached on Monday - Friday, 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



NHAN T. TRAN
Patent Examiner